REMARKS

Claims 1-24 are pending in the application.

Claims 1-4, 10-16, and 22-24 have been rejected.

Claims 5-9 and 17-21 have been objected to as depending from rejected claims.

Claim 11 has been amended to correct informalities.

The specification has been amended, as indicated above, to correct minor informalities.

No new matter has been added.

Reconsideration of the Claims is respectfully requested.

1. Objection to the Claims

Claim 11 was objected to due to informalities. Appropriate correction has been made.

2. Rejection under 35 U.S.C. § 102

Claims 1-4, 10-16, and 22-24 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Application No. 2003/0035445 to Choi ("Choi").

For establishing anticipation, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. . . . The identical invention must be shown in as complete detail as is contained in the . . . claim." MPEP § 2131 at p. 2100-73 (8th ed., rev. 3, August 2005) (citations omitted).

Choi relates to "a cost effective way for communicating both Ethernet and PDH/SDH/SONET data using time division multiplexing techniques. The integrated Ethernet and PDH/SDH/SONET communication system time division multiplexes PDH/SDH/SONET data with Ethernet data and transmits and receives the combined data stream using Ethernet-based communication technology." (Choi ¶ 0005). As noted in the Office Action, Choi recites a decoder/encoder before prior to a multiplexer/demultiplexer, which may also follow the multiplexer/demultiplexer. (*Cf.* Choi Figs. 1 & 4). Choi, however, does not show a *signal conditioning circuit* as set out in Applicant's application. The decoder/encoder of Choi instead "encodes and decodes the Ethernet and PDH/SDH/SONET *data for communication*." (Choi ¶ 0005). Further, Choi, as understood, does not recite operations with respect to "bit streams" because of the inclusion of serializer/deserializer. The serializer/deserializer "converts the parallel data into serial data and vice versa." (Choi ¶ 0005).

As explained in Applicant's specification, the "*signal conditioning circuits* within the high-speed bit stream interface modules operate to condition their serviced signals to compensate for the manner in which these signal paths affect the serviced signals. The manner in which the signal paths affect the serviced signals may differ from signal path to signal path in a particular application and/or in differing applications." (Specification at page 17, lines 6-10).

Independent claim 1 recites, *inter alia*, a "high-speed serial bit stream interface module comprising: a line side interface that services a line side media, that receives a line side receive signal, and that transmits a line side transmit signal; a board side interface that services a plurality of transmit bit streams and a plurality of receive bit streams; at least one multiplexer that multiplexes the plurality of transmit bit streams to produce the line side transmit signal; at least one demultiplexer that demultiplexes the line side receive signal to produce the plurality of receive bit streams; and *a plurality of signal conditioning circuits, each of which services a respective bit stream of the plurality of transmit bit streams and the plurality of receive bit streams*." (emphasis added).

Independent claim 13 recites, *inter alia*, a "high-speed serial bit stream interface module comprising: a *back plane/box interface* that services a first plurality of transmit bit streams and a first plurality of receive bit streams; a board side interface that services a second plurality of transmit bit streams and a second plurality of receive bit streams; at least one demultiplexer that demultiplexes the *first plurality of receive bit streams* to produce *the second plurality of receive bit streams*; at least one multiplexer that multiplexes the *second plurality of transmit bit streams* to produce the *first plurality of transmit bit streams*; and *a plurality of signal conditioning circuits*, each of which services a respective bit stream of the first plurality of transmit bit streams and the first plurality of receive bit streams."

Accordingly, Applicant respectfully submits that each and every element of its claimed invention is not found in Choi. Further, that Applicant's claimed invention is not shown in as complete detail as the device of Choi. In this regard, Choi does not anticipate Applicant's Claim 1 and Claims 2-4 and 10-12 that depend directly or indirectly therefrom, and does not anticipate Applicant's Claim 13 and Claims 14-16 and Claims 22-24 that depend directly or indirectly therefrom.

3. Allowable Subject Matter

Claims 5-9 and 17-21 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant notes with appreciation this indication of allowability.

4. Conclusion

As a result of the foregoing, the Applicant respectfully submits that claims 1-24 in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ksmith@texaspatents.com.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Garlick Harrison & Markison Deposit Account No. 50-2126.

Respectfully submitted,

Date: January 22, 2007

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